DIGITAL COMPUTER NEWSLETTER

The purpose of this newsletter is to provide a medium for the interchange, among interested persons, of information concerning recent developments in various digital computer projects

OFFICE OF NAVAL RESEARCH • MATHEMATICAL SCIENCES DIVISION

Vol. 3, No. 3* October 1951

NAVEXOS-P-645

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GENERAL PURPOSE COMPUTERS

The Circle Computer

The Circle Computer is a fully electronic selective sequence machine designed for low cost quantity production. In logical conception it is nearly identical with the digital computer at the Princeton Institute for Advanced Study; the same single address orders are used. In order to simplify the construction and minimize the cost, there has been a sacrifice in speed relative to the Princeton machine.

The Circle Computer uses a magnetic drum memory with a capacity of 1024 words of 40 binary digits each. The average multiplication time, including access, is 50 milliseconds; the average addition time is 25 milliseconds.

A developmental model is nearing completion at the Physics Department of Washington Square College, New York University.

Further information is available from the designer (Nuclear Development Associates of White Plains, New York), or the manufacturer (Hogan Laboratories of New York City).

*The July 1951 issue of the Digital Computer Newsletter should be corrected to read Vol. 3, No. 2.

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Naval Proving Ground Calculators

The Aiken Relay Calculator (Mark II) is now being operated six days a week, 24 hours a day. During the past six months a variety of problems have been treated including determination of characteristic roots of two 18 x 18 matrices, a cavitation problem involving complex integration, and various items relating to ballistic research as well as the preparation of various ballistic and lead angle tables. An additional experimental checking circuit has been installed to bring the machine closer to a completely automatic checked machine.

The Mark III Calculator is also being operated six days a week, 24 hours a day. The relative per cent of good running time is still considerably under that of the Mark II but gradually improving. The machine has been successfully used on various test problems as well as on a considerable amount of production work. Two sets of computation were produced for a fire control system which resulted in over 1000 printed pages of output. In addition to this, several hundred trajectories were integrated in connection with a general ballistic table; and one short problem which involved the generation and use of random numbers was successfully completed.

Aberdeen Proving Ground Computers

The effective operating percentage for the Eniac for the period 1 July 1950 through 30 June 1951 was 60%. Operating time lost putting problems on the machine, checking programming, performing data analyses, and down time due to human operating error accounted for 16% of the period. The remaining 24% was spent locating and correcting machine errors, non duplication time, and preventive maintenance. The Eniac is operated 24 hours each day from 0800 Monday through 2400 on Friday.

During the period 1 March through 31 July 1951, the Eniac has completed computations for 24 different problems (which involved 53 changes of program), dealing with such varied topics as:

a. data reduction,

b. firing tables and bombing tables,

c. supersonic airflow,

d. crystal structure,

e. heat flow,

f. trend analysis, and

g. weather forecasting.

The Automatic Printing Calculator, a product of the Benson-Lehner Corporation, was installed immediately after its arrival from the West Coast, and is now operating satisfactorily.

This Calculator consists of an automatic Friden desk computer and an electric IBM typewriter, both of which have been slightly modified so as to enable them to operate in tandem.

Electronic Computer Corporation Computers

The Electronic Computer Corporation, 265 Butler Street, Brooklyn 17, New York, is currently constructing three magnetic drum computers. One of these is primarily a special purpose data handling machine intended for use in mechanizing the handling of subscriptions for a large weekly magazine. This machine was contracted for in the fall of 1950 and is scheduled for delivery in the latter part of 1952. The second computer under way is a general purpose mathematical machine with 10,000 word memory and punched card input and output which is being built for the Department of the Army. It was contracted for in July 1951 and is also scheduled for delivery in late 1952. The third computer is a general purpose mathematical machine intended as a prototype of a moderate cost digital computer suitable for general use wherever extreme speed is not of prime importance.

This last machine is provided with typewriter input and printing and with magnetic tape as an auxiliary memory. The internal memory consists of 512 words each 36 binary digits in length with

an average access time of 10 milliseconds. The computer contains approximately 100 tubes and 1500 germanium diodes. The computer size and power requirements are sufficiently low to permit mounting on casters and use of a plug-in line cord thus avoiding need for permanent installation and permitting locating as desired.

The ORDVAC

The control of the ORDVAC has been tested by using order pairs in a repetitive way for most of the orders. More recently, the memory has been tested for read-around-ratios. This work has been carried out by using a routine which requires the operation of most of the computer and checks the read-around-ratio on every cathode ray tube in certain specified addresses. The read-around-ratios are then printed out on the teletype page printer. This has shown that the read-around-ratio is in excess of 50 on about 12 of 40 tubes. Work is now continuing at Illinois in an effort to improve the read-around-ratio.

The SEAC

At the National Bureau of Standards a collaborative program is under way; staff members of the NBS Electronic Computers Laboratory are cooperating with representatives of two other groups which plan to construct computers based on the SEAC design. These two groups are (1) the Joint Long Range Proving Ground of the USAF, and (2) the University of Michigan group engaged in a research program for the USAF. Because of the SEAC's performance record and flexible design, these groups initiated a program to develop a modified version of the SEAC design particularly suited to their requirements. For example, the modified design will incorporate a rotating drum as well as a high-speed acoustic memory.

The expansion of SEAC has continued and most of the features of the maximum design are installed and in trial operation. The maximum SEAC design incorporates (for experimental purposes) both an acoustic delay line memory and an electrostatic Williams tube memory, as well as a wide variety of high-speed input-output equipment, all of which are in use. The "Automonitor" feature, which causes the machine to print out each instruction and the result of its execution, has been installed and is in trial use. The maximum design also contains provision for two distinct modes of operation of the control,--a four-address system or a three-address system. The latter feature is currently being realized at NBS. Associated with the three-address system, a special Floating Address feature will be available to automatize certain programming operations involved in reutilizing standard sub-routines.

The SWAC

The 5JP11A and 5JP1A tubes used in the SWAC all have flaws which will not store dashes. Selection was used to hold this fault to a minimum but the average tube has at least four flaws which will not store dashes, and many more blemishes which produce smaller than ordinary dash signals.

None-the-less some computing on actual problems can be done, and at any given time small problems can be run; however, problems using the full memory require very careful centering adjustments, and long term drift in d.c. voltages makes repeated readjustments necessary.

Most blemishes under repeated high duty factor use produce smaller and smaller signals, but after minutes of such bombardment a partial recovery is made. The Institute for Numerical Analysis is encouraging the Engineering Department of UCLA to start a study of these blemishes.

An optical tape reader unit is almost ready for use, and components for the magnetic tape reader are under construction. More effort will be put on the magnetic drum in the near future.

The Raytheon Computer

The clock, central control, main memory, hunt and one external memory rack are now in the system testing phase. The problem preparation units and output printer are undergoing test and should be completed in September. The operator's console has been built; its contents to be unit tested in September. Fabrication of the arithmetic unit is nearing completion and sub-system testing of many of the arithmetic unit chassis is continuing. With system testing of this unit expected

to be completed in October, it is anticipated that operational testing of the entire machine will proceed at that time.

The University of Toronto Electronic Computer UTEC

The Computation Centre is maintained at the University of Toronto by grants from the National Research Council and the Defense Research Board of Canada for carrying out computations by modern methods. Towards this end a small high-speed electronic computer is under construction. This computer has a 512 word, twelve binary digit, electrostatic memory, an electronic arithmetic and control section, and Flexowriter paper tape input-output. Later a Raytheon magnetic tape drive mechanism will be incorporated as an auxiliary memory.

The arithmetic unit and control have been completed for over a year. With the help of a seven word toggle switch memory and a single word flip-flop register, elaborate cycling tests have been performed, utilizing all of the eight orders the machine can perform, except input and output. The Williams tube type storage contains twelve 3" cathode ray tubes and has performed satisfactorily in the required operations of storing, reading, and writing. At present the arithmetic control and storage units are being tested together. Breadboard models of the circuits for loading and unloading the computer with the Flexowriter equipment have been tested, and the final equipment for this purpose is under construction.

It is planned to start the construction of a full scale computer shortly, with its main features similar to those of the model.

The Ferranti Computer at Manchester University, England*

During the week of July 9, the University of Manchester held an inaugural conference celebrating the completion and installation of its new high-speed electronic computing machine. This machine was built for the University by Ferranti, Ltd., and uses commercially engineered components but follows the design developed at the University. As such, it is the first commercially available automatic high-speed computer in Europe, and the first one on the market generally to include an electrostatic memory. At present, two additional machines are being built by Ferranti, of which one, for the use of Ministry of Supply agencies and to be located at the Armament Research Establishment, Fort Halstead, is almost completed. The other one is expected to remain at Ferranti's to assist their staff in further research and development.

A more complete description, together with a broad outline of prospective of the machine computing program, will be found in Nature 168, 95 (1951). Some of the points bear stressing in comparison with American computer designs. One of these is the basic pulse rate of 100 kilocycles, rather than the megacycle rate of U. S. machines employing electrostatic storage. The components are therefore operating for the most part comfortably within their designed ranges, and it was felt unnecessary to make provisions for marginal checking. Even more important is the structure of the internal memory around which the machine is built. The difficulties arising from the nearly two orders of magnitude difference in access speed between the Williams tube storage and the magnetic drum backing it up are greatly reduced by making transfers infrequently and then only in quanta of an entire tube's worth of information (1280 binary digits, equivalent to the contents of half a track on the drum). Access time to the electrostatic memory is governed by the latter's regeneration rhythm which controls the operation of the entire machine. Consecutive periods of 240 microseconds each are used alternatively for regeneration of the information in the memory tubes and for reading information out of or into them. The regeneration periods are used to scan in orderly fashion half-line after half-line, taking 256 such periods to make one complete round of the store. Since information becomes available in groups of 20 bits, rather than complete words of 40 digits, the operating rhythm of the machine is one of "bars" each containing four "beats" of which two are used for scanning and two for action. In this respect the Ferranti machine differs from the prototype whose basic bar contained two beats of 450 microseconds each, allowing to scan or to process an entire line at a time.

In all of these respects the design has sacrificed computing speed for engineering ease and reliability. A notable and successful exception is the multiplier, which at a deliberate increase in

* EUROPEAN SCIENTIFIC NOTES 1 August 1951

complexity of design achieves a multiplication time but little more than twice the addition time. Multiplication is effected by accumulating simultaneously as many multiplicands as there are ones in the multiplier, each delayed by as many pulse lengths as the position of the one to which it corresponds indicates. Thus machine time for a problem can no longer be estimated exclusively in terms of the number of multiplications required.

The machine has been in operation during the past month on a wide variety of test problems and its reliability has been steadily improving. With the early elimination of errors due to drifting adjustments, especially in the cathode ray tube storage, the one remaining serious cause of malfunctioning is the failure of tubes, now occurring about two or three times a week. A further reduction by one or two orders of magnitude in this failure rate is anticipated as the first generation of tubes, maltreated during early test runs, is eliminated. In addition a test procedure has been developed which, in case of a tube failure in the arithmetic units, especially the multiplier, will stop the machine and lead to the identification of the faulty tube. Considerable facilities for manual interference and inputs, optional stops and monitoring tubes are provided on the console allowing an error analysis right on the machine.

COMPONENT DEVELOPMENTS

The Computer Research Corporation

The Computer Research Corporation, 1954 Carson Street, Torrance, California, has announced the availability of a minature magnetic recording head and a Ferro-Resonant Flip-Flop to replace vacuum tubes in certain counting, amplifying and control applications. Further information can be obtained by writing the corporation.

Physical Research Laboratories Computer Development

Among other activities, the Physical Research Laboratories, 542 North Fair Oaks Avenue, Pasadena 3, California, has produced a magnetic drum memory, which is said to be available commercially, and a pulse transformer, which has been produced in pilot quantities. The memory drum, which is 6-1/2 inches in diameter and 10 inches long, is driven at 6000 rpm. The memory head, a development of the laboratories, is based on a torriodally wound mu-metal ribbon core. Although the read-write speed on the drum is 400 kc per second, it is not recommended that it be used much above 200 kcps as a square-wave device. The memory has operated at cell densities of 200 per inch and is satisfactory well above a 100 per inch.

The Company claims very fast characteristics for the minature pulse transformer. For example, when used as a triggered blocking oscillator transformer, it has a pulse-rise time of 5 millimicroseconds and a pulse duration of 20 millimicroseconds, yet as a coupling transformer will hold up 95% for 5 microseconds. While these properties are not essential when used as a pulse-follower in computer circuitry, they are none-the-less desirable.

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Comments, letters to the editor, and additional contributions for inclusion in the Newsletter should be addressed to:

Code 434
Office of Naval Research
Navy Department
Washington, D. C.